UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/031,326	02/26/1998	JOSEPH J. KARNIEWICZ	303.376US1	8474

21186 7590 01/29/2004

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
PHAN, THAI Q	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 01/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/031,326	Joseph J. Karniewicz
Examiner	**Art Unit**
Thai Phan	2128

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Nov. 17, 2003*.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-36* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This Office Action is in response to applicant's amendment filed on Nov. 17, 2003. Claims 1-36 are now pending.

Specification

1. The attempt to incorporate subject matter into this application by reference to a co-pending and co-assigned is incomplete because it does not provide current status and complete US patent application Serial Number for the record.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Madhavan et al., US patent no. 5,675,545, in views of Ho, William, US patent no. 6,421,814 B1 ('814) and Ho et al, US patent 6.009,251 ('251).

As per claims 1 and 9, Madhavan discloses a cell design method and design system for designing and testing semiconductor memory with feature limitations substantially similar to the claimed invention (Abstract and "Summary of the Invention"). According to Madhavan, the

design apparatus includes global files for global variables and design data relating to layout or schematics layout and connectivity data of the functional block, a plurality of cell configuration files or claimed local files, each relating a plurality of local variables to the global variables in system files (Figs. 9, 10-11, col. 2, lines 27-44, col. 5, line 50 to col. 6, line 47, col. 8, lines 31-50, for example), and a plurality of cells, each cell corresponding to a local file and having a set of parameters derived by relating the local variables to the global variables in the global source files such that the changes of global variables in the global files reflect or may cause changes in the programmable cells, including layout of the hierarchical semiconductor structure in accordance with parameters in the local files (Figs. 5-10, col. 6, line 48 to col. 8, line 50). Madhavan does not expressly disclose geometric variables related to physical layout in a hierarchical manner as claimed.

Practitioner in the art at the time of the invention was made would have found Madhavan physical semiconductor memories in the integrated circuit area could have geometric shapes or sizes taking geometric parameter values, occupied in the chip placement area such that the hierarchical placement of cells is on the semiconductor substrate. Such geometrical feature in the semiconductor circuit cell layout is also well-known in the semiconductor circuit design. In fact, Ho ('814) teaches geometrical layout variables or parameters and such relations in geometrical layout data for physical design with faster and better layout in integrated circuit design (Background of the Invention, col. 1, lines 48-60, Fig. 1B, col. 5, lines 33-60). Ho ('251) also teaches a net list for geometry and subcell design with local geometry and parent references for hierarchical cell layout design and cell interconnection verification (Figs. 2-4, col. 3, lines 25-67,

col. 7, lines 7-36, col. 8, line 29 to col. 10, line 43, for example) in order to reduce verification time for cell layout as taught in Ho.

This would motivate practitioner in the art at the time of the invention was made to use Ho teaching of geometrical layout variables in hierarchical relationships for physical design of the integrated circuit as disclosed in Madhavan to improve layout processing time and faster in circuit design verification and testing as in Madhavan.

As per claims 2-3 and 10-11, Madhavan discloses local files would obviously include inherent file from source files, instance files, data files, etc. (Figs. 9-11).

As per claim 4, Madhavan discloses master files in hierarchical design acting as initial version of a corresponding local file for design, modification, increment compilation, etc.

As per claim 5, Madhavan discloses file or clean sheet file for containing design rules for a plurality of cells for coordinated design as claimed.

As per claim 6, Madhavan discloses file extraction and related variable extraction for design and update design.

As per claims 7-8, Madhavan discloses the design display in local host for display interactively interface.

As per claim 12, Madhavan discloses file update including update global file for coordinate process.

As per claim 13, Madhavan discloses local display in local user workstation for the design process.

As per claim 14, Madhavan discloses computer program in concurrent with design program for circuit design process as claimed.

As per claim 15, Madhavan discloses a method and design system for designing and testing semiconductor memory with feature limitations substantially similar to the claimed invention (Abstract and "Summary of the Invention"). According to Madhavan, the design apparatus includes global files for global variables and design data relating to layout or schematics layout and connectivity data of the functional block, a plurality of cell configuration files or claimed local files, each relating a plurality of local variables to the global variables in system files (Figs. 9, 10-11, col. 2, lines 27-44, col. 5, line 50 to col. 6, line 47, col. 8, lines 31-50, for example), and a plurality of cells, each cell corresponding to a local file and having a set of parameters derived by relating the local variables to the global variables in the global source files such that the changes of global variables in the global files reflect or may cause changes in the programmable cells, including layout of the hierarchical semiconductor structure in accordance with parameters in the local files (Figs. 5-10, col. 6, line 48 to col. 8, line 50). Madhavan does not expressly disclose geometric variables related to physical layout in hierarchical manner as claimed.

Practitioner in the art at the time of the invention was made would have found Madhavan physical semiconductor memories in the integrated circuit area could have geometric shapes or sizes taking geometric parameter values, occupied in the chip area for cell placement design. Furthermore, such geometrical feature in the semiconductor circuit cell layout is also well-known in the semiconductor circuit design. In fact, Ho ('814) teaches geometrical layout variables or

parameters and such relations in geometrical layout data for physical design with faster and better layout in integrated circuit design (Background of the Invention, col. 1, lines 48-60, Fig. 1B, col. 5, lines 33-60). Ho ('251) also teaches the circuit net list for geometry and subcell design with local geometry and parent references for hierarchical cell layout design and cell interconnection verification (Figs. 2-4, col. 3, lines 25-67, col. 7, lines 7-36, col. 8, line 29 to col. 10, line 43, for example) in order to reduce verification time for cell layout as taught in Ho.

This would motivate practitioner in the art at the time of the invention was made to use Ho teaching of geometrical layout variables in hierarchical relationships for physical design of the integrated circuit as disclosed in Madhavan to improve circuit layout processing time and to improve design and verification as in Madhavan circuit design and testing.

As per claims 16-21, similarly, with the rejection rationale above, the claims are also rejected due to its similarities to claims 2-8 and claims 11-14.

As per claim 22, Madhavan a discloses method and design system for designing and testing semiconductor memory with feature limitations substantially similar to the claimed invention (Abstract and "Summary of the Invention"). According to Madhavan, the design apparatus includes global files for global variables and design data relating to layout or schematics layout and connectivity data of the functional block, a plurality of cell configuration files or claimed local files, each relating a plurality of local variables to the global variables in system files (Figs. 9, 10-11, col. 2, lines 27-44, col. 5, line 50 to col. 6, line 47, col. 8, lines 31-50, for example), and a plurality of cells, each cell corresponding to a local file and having a set of parameters derived by relating the local variables to the global variables in the global source

files such that the changes of global variables in the global files reflect or may cause changes in the programmable cells, including layout of the hierarchical semiconductor structure in accordance with parameters in the local files (Figs. 5-10, col. 6, line 48 to col. 8, line 50). Madhavan does not expressly disclose geometric variables related to physical layout in hierarchical manner as claimed.

Practitioner in the art at the time of the invention was made would have found Madhavan physical semiconductor memories in the integrated circuit area could have geometric shapes or sizes taking geometric parameter values, occupied in the chip area for hierarchical cell placement design. Such geometrical feature in the semiconductor circuit cell layout is also well-known in the semiconductor circuit design. In fact, Ho ('814) teaches geometrical layout variables or parameters and such relations in geometrical layout data for physical design with faster and better layout in integrated circuit design (Background of the Invention, col. 1, lines 48-60, Fig. 1B, col. 5, lines 33-60). Ho ('251) also teaches net list for geometry and subcell design with local geometry and parent references for hierarchical cell layout design and cell interconnection verification (Figs. 2-4, col. 3, lines 25-67, col. 7, lines 7-36, col. 8, line 29 to col. 10, line 43, for example) in order to reduce verification time for cell layout as taught in Ho.

This would motivate practitioner in the art at the time of the invention was made to use Ho teaching of geometrical layout variables in hierarchical relationships for physical design of the integrated circuit as disclosed in Madhavan to better improve and faster layout processing in circuit design and testing as in Madhavan.

As per claims 23-24, Madhavan discloses inherent design file, and instance file in the design database.

As per claim 25, Madhavan disclosure would imply design framework for use in the chip design process. Such design framework could include not limited to CADENCE functional design system as claimed.

As per claims 26, 29, and 33, Madhavan discloses method and design system for designing and testing semiconductor memory with feature limitations substantially similar to the claimed invention (Abstract and "Summary of the Invention"). According to Madhavan, the design apparatus includes global files for global variables and design data relating to layout or schematics layout and connectivity data of the functional block, a plurality of cell configuration files or claimed local files, each relating a plurality of local variables to the global variables in system files (Figs. 9, 10-11, col. 2, lines 27-44, col. 5, line 50 to col. 6, line 47, col. 8, lines 31-50, for example), and a plurality of programmable cells (Background of the Invention), each cell corresponding to a local file and having a set of parameters derived by relating the local variables to the global variables in the global source files such that the changes of global variables in the global files reflect or may cause changes in the programmable cells, including layout of the hierarchical semiconductor structure in accordance with parameters in the local files (Figs. 5-10, col. 6, line 48 to col. 8, line 50). Madhavan does not expressly disclose geometric variables related to physical layout in hierarchical manner as claimed.

Practitioner in the art at the time of the invention was made would have found Madhavan physical semiconductor memories in the integrated circuit area could have geometric shapes or

sizes taking geometric parameter values, occupied in the chip area for hierarchical physical design. Such geometrical feature in the semiconductor circuit cell layout is also well-known in the semiconductor circuit design. In fact, Ho ('814) teaches geometrical layout variables or parameters and such relations in geometrical layout data for physical design with faster and better layout in integrated circuit design (Background of the Invention, col. 1, lines 48-60, Fig. 1B, col. 5, lines 33-60). Ho ('251) also teaches the net list for geometry and subcell design of the circuit with the local geometry and parent references for hierarchical cell layout design and cell interconnection verification (Figs. 2-4, col. 3, lines 25-67, col. 7, lines 7-36, col. 8, line 29 to col. 10, line 43, for example) in order to reduce verification time for cell layout as taught in Ho.

This would motivate practitioner in the art at the time of the invention was made to use Ho teaching of geometrical layout variables in hierarchical relationships for physical design of the integrated circuit as disclosed in Madhavan to better improve and faster layout processing in circuit design and testing as in Madhavan.

As per claims 27 and 28, Madhavan discloses global files and related parameters files in the semiconductor memory design. Such design parameter files could include inherent files and instance files as claimed.

As per claim 29, Madhavan and Ho disclose means for displaying design process.

As per claim 31, Madhavan discloses update design data in database spreadsheet such as in cleansheet file (col. 7, lines 1-5, for example).

As per claim 32, Madhavan discloses the display means for value changes, design files, and means for allowance of user interface.

As per claims 34-36, Madhavan disclosure could include the claimed limitations in the parametric design process.

Response to Arguments

4. Applicant's arguments filed June 30, 2003 have been fully considered but they are moot in view of a new ground of rejection.

In response to applicant's argument Madhavan and Ho ('814) fail to disclose or teach geometric variables related to the physical layout of a hierarchical semiconductor structure as recited in the claims (pages 10-12), the examiner agrees with. Such argued feature is however known in the art. In fact, Ho (251) teaches cell placement layout design verification. Ho teaches the layout design in hierarchical semiconductor structure with netlist for subcells and parent cell placement and interconnection information. The cell placement information includes cell geometrical variables on the hierarchical semiconductor substrate and placement interrelation between cells for a complete cell placement design (cols. 7-13).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. US patent no. 6,249,902 B1, issued to Igusa et al., on June 2001.
2. US patent no. 6,011,911, issued to Ho et al, on Jan. 2000

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Thai Phan whose telephone number is (703) 305-3812.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703)305-3900.

Any response to this action should be mailed to:

Commissioner of Patents

P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to:

(703) 872-9306, (for formal communications intended for entry)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

January 23, 2004

Thai Phan
Patent Examiner
AU: 2128